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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,001	12/30/2003	Sung-Kwon Lee	51876P507	9960

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EXAMINER	
JEFFERSON, QUOVAUNDA	

ART UNIT	PAPER NUMBER
2823	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,001	LEE ET AL.	
	Examiner	Art Unit	
	Quovaunda Jefferson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20,31,32 and 36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20,31,32 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 27, 2007 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5, 9-14, 18-20, 31, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicant's Admitted Prior Art (herein referred to as "AAPA").

Regarding claim 1, AAPA discloses a method for fabricating a semiconductor device, comprising the steps of forming an etch stop layer **S** having a multi-layer structure along a profile containing conductive patterns **G** formed on a substrate, etching selectively a first inter-layer insulation layer **14** deposited on the etch stop layer and the etch stop layer to form a first contact hole exposing a surface of the substrate allocated between the conductive patterns (Figure 1A), forming a first plug **17** by depositing a conductive layer on an entire surface of the resulting structure containing the first contact hole and planarizing the conductive layer, the first inter-layer insulation layer and the etch stop layer at the same plane level of the conductive patterns (Figure 1B), performing a cleaning process to remove remnants from the planarization process (page 5, lines 6-19), forming an attack barrier layer **18** on an entire surface of a resulting structure, wherein the attack barrier layer removes a plurality of gaps in the etch stop layer which occurs during the planarization process and the cleaning process (figure 1C), etching selectively a second inter-layer insulation layer **18, 19** deposited along a profile containing the first plug to form a second contact hole exposing the first plug (Figure 1C); and forming a second plug **22** electrically connected to the first plug through the second contact hole (Figure 1D).

Regarding claim 2, AAPA teaches the multilayer structure of the etch stop layer includes nitride layers as top and bottom most layers and at least one insulating material-based layer being disposed between the nitride layer and having a lower dielectric constant than those of the nitride layers (page 2, line 22).

Regarding claim 3, AAPA teaches the first inter-layer insulation layer and the etch stop layer disposed on an upper surface of each conductive pattern are etched by performing one of a plasma etching process with use of a mask opening only a cell region and a CMP process prior to the step of performing the SAC etching process for forming the first contact hole (page 4, lines 1-25).

Regarding claim 5, AAPA teaches after the step of performing the cleaning process, the attack barrier layer **18** is deposited on an entire surface of the profile containing the first plug (figure 1C).

Regarding claim 9, AAPA teaches the insulating material-based layer having a lower dielectric constant than those of the nitride layers uses one of an oxide-based layer, an aluminum oxide (Al_2O_3) layer and a tantalum oxynitride (TaON) layer (page 2, line 22).

Regarding claim 10, AAPA teaches the cleaning process uses a cleaning solution of hydrofluoric acid (HF) or buffered oxide etchant (BOE) (page 5, lines 19).

Regarding claim 11, AAPA teaches the conductive pattern **G** is a gate electrode pattern and the second plug **22** is a storage node contact plug (page 2, line 26 and page 8, line 9).

Regarding claim 12, AAPA teaches a method for fabricating a semiconductor device, comprising the steps of forming an etch stop layer **S** having a multi-layer structure along a profile containing conductive patterns **G** formed on a substrate, etching selectively a first inter-layer insulation layer **14** deposited on the etch stop layer and the etch stop layer to form a first contact hole exposing a surface of the substrate allocated between the conductive patterns (figure 1A), forming a first plug **17** by depositing a conductive layer on an entire surface of a structure containing the first contact hole and planarizing the conductive layer, the first inter-layer insulation layer, and the etch stop layer at the same plane level of the conductive patterns (figure 1B), performing a cleaning process to remove remnants from the planarizing process (page 5, lines 6-19), forming an attack barrier layer **18** on an entire surface of a resulting structure including the first plug, the conductive patterns, and the etch stop layer, wherein the attack barrier layer removes a plurality of gaps which occur during the planarizing process and the cleaning process (figure 1C), forming a second inter-layer insulation layer **18, 19**, etching selectively the second inter-layer insulation layer **18, 19** formed on the attack barrier layer and the attack barrier layer to form a second contact hole exposing the first plug (figure 1C), and
forming a second plug **22** electrically connected to the first plug through the second contact hole (figure 1D).

Regarding claim 13, AAPA teaches the multilayer structure of the etch stop layer includes nitride layers as top and bottom most layers and at least one insulating

material-based layer being disposed between the nitride layer and having a lower dielectric constant than those of the nitride layers (page 2, line 22).

Regarding claim 14, AAPA teaches the first inter-layer insulation layer and the etch stop layer disposed on an upper surface of each conductive pattern are etched by performing one of a plasma etching process with use of a mask opening only a cell region and a CMP process prior to the step of performing the SAC etching process for forming the first contact hole (page 4, lines 1-25).

Regarding claim 18, AAPA teaches the insulating material-based layer having a lower dielectric constant than those of the nitride layers uses one of an oxide-based layer, an aluminum oxide (Al_2O_3) layer and a tantalum oxynitride (TaON) layer (page 2, line 22).

Regarding claim 19, AAPA teaches the cleaning process uses a cleaning solution of hydrofluoric acid (HF) or buffered oxide etchant (BOE) (page 5, lines 19).

Regarding claim 20, AAPA teaches the conductive pattern **G** is a gate electrode pattern and the second plug **22** is a storage node contact plug (page 2, line 26 and page 8, line 9).

Regarding claim 31, AAPA teaches the second inter-layer insulation layer has a flow-fill property (page 4, line 22 to page 5, line 11).

Regarding claim 32, AAPA teaches the second inter-layer insulation layer is made of an oxide-based material selected from a group consisting of advanced planarization layer (APL), spin on dielectric (SOD), spin on glass (SOG) and borophosphosilicate glass (BPSG) (page 4, line 22 to page 5, line 11).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4, 8, 15, 17, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art.

Regarding claims 4 and 15, AAPA fails to teach the thickness of the first inter layer insulation layer and the etch stop layer disposed on each conductive pattern ranges from about 500 Angstroms to about 1500 Angstroms.

However, given the teaching of the references, it would have been obvious to determine the optimum thickness of the semiconductor layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Regarding claims 8 and 17, AAPA fails to teach the attack barrier layer has a thickness ranging from about 50 Angstroms to about 500 Angstroms.

However, given the teaching of the references, it would have been obvious to determine the optimum thickness of the semiconductor layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Regarding claim 36, AAPA fails to teach the second inter-layer insulation layer has a thickness ranging from about 1000 Angstroms to about 8000 Angstroms.

However, given the teaching of the references, it would have been obvious to determine the optimum thickness of the semiconductor layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the

data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Claims 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA as applied to claim 1 above, and further in view of Tran.

Regarding claim 6, AAPA fails to teach after the step of forming the second contact hole, the attack barrier layer is formed along a profile containing the second contact hole.

Tran teaches after the step of forming the second contact hole (in layer **64**), the attack barrier layer **67** is formed along a profile containing the second contact hole (figure 6 and column 6, lines 37-40) because the barrier layer serves as an adhesion promoter for the conductive plug material to be added and prevents the reaction of the conductive plug and the semiconductor layers.

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Tran with that of AAPA because the barrier layer serves as an

adhesion promoter for the conductive plug material to be added and prevents the reaction of the conductive plug and the semiconductor layers.

Claims 7 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA as applied to claims 1 and 12 above, and further in view of Zhang et al, US Patent Application Publication 2001/0014496.

Regarding claim 7 and 16, AAPA fails to teach the attack barrier layer is a nitride-based layer.

Zhang teaches the attack barrier layer is a nitride-based layer [0094] because the use of a silicon nitride film for the interlayer insulating film is advantageous in that hydrogen and other contaminants does not effuse from the active region of the TFTs in the peripheral circuit region or permit contaminants to reach the TFT, thereby degradation of the semiconductor device.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Zhang with that of AAPA because the use of a silicon nitride film for the interlayer insulating film is advantageous in that hydrogen and other contaminants does not effuse from the active region of the TFTs in the peripheral circuit region or permit contaminants to reach the TFT, thereby degradation of the semiconductor device.

Response to Arguments

Applicant's arguments with respect to claims 1-20, 31, 32, and 36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 7AM to 3:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

QVJ

QVJ

FERNANDO L. TOLEDO
PRIMARY PATENT EXAMINER